ESP-32S Datasheet

October 3, 2016

Disclaimer and Copyright Notice.

Notice

Product version upgrades or other reasons, possible changes in the contents of this manual. AI-Thinker reserves in the absence of any notice or indication of the circumstances the right to modify the content of this manual. This manual is used only as a guide, Ai-thinker make every effort to provide accurate information in this manual, but Ai-thinker does not ensure that manual content without error, in this manual all statements, information and advice nor does it constitute any express or implied warranty.

Contents

List of Tables

List of Figures

1.Preface

ESP-32S is a powerful, generic WiFi-BT-BLE MCU module that targets a wide variety of applications ranging from low power sensor networks to the most demanding tasks such as voice encoding, music streaming and MP3 decoding.

At the core of this module is the ESP32 chip, which is designed to be scalable and adaptive. There are 2 CPU cores that can be individually controlled or powered, and the clock frequency is adjustable from 80 MHz to 240 MHz. The user may also power off the CPU and make use of the low power coprocessor to constantly monitor the peripherals for changes or crossing of thresholds. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, low noise sense amplifiers, SD card interface, Ethernet, high speed SDIO/SPI, UART, I2S and I2C.
The integration of Bluetooth, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted,and that it is future proof: using Wi-Fi allows a large physical range and direct connection to the internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 μA, making it suitable for battery powered and wearable electronics applications. ESP-WROOM-32 supports data rates up to 150 Mbps, and 22 dBm output power at the PA to ensure the widest physical range. As such the chip does offer industry leading specifications and the best optimized performance for electronic integration, range and power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LWIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that developers can continually upgrade their products even after their release. The software releases are covered under the ESP32 bug bounty program nd any bugs can be reported to bugbounty@espressif.com. As the SDK of ESP-32S or ESP32 is opensource, the user can build his own platforms and operating systems. For more in-depth discussion of this, the developer can contact john.lee@espressif.com.

ESP-32S has AI-Thinker's long term support — ESP32 will be covered under Espressif's longevity program and be available for the next 12 years. The design of ESP-32S will be open-source when it has been fully optimized. Feedbacks about the module, chip, API or firmware can be sent to Support@aithinker.com.

Table 1 provides the specifications of ESP-32S.

Table 1 ESP-32S Specifications

Categories	Items	Values
WiFi	Standards	
	Protocles	802.11 b/g/n/d/e/i/k/r (802.11n up to 150 Mbps)
	Frequency Range	2.4GHz-2.5GHz (2400M-2483.5M)
Bluetooth	Protocols	Bluetooth v4.2 BR/EDR and BLE specification
	Radio	NZIF receiver with -98 dBm sensitivity
		Class-1, class-2 and class-3 transmitter
		AFH
	Audio	CVSD and SBC
Hardware	Module interface	SD card, UART, SPI, SDIO, I2C, LED PWM, Motor PWM, I2S, I2C, IR
		GPIO, capacitive touch sensor, ADC, DAC, LNA pre-amplier
	On-chip sensor	3.0~3.6V
	On-board clock	Average value: 80mA
	Operating voltage	-40°~125°
	Operating current	Normal temperature
	Operating temperature range	14.3mm*24.8mm*3mm
	Ambient temperature range	N/A
	Package size	
Software	Wi-Fi mode	Station/softAP/SoftAP+station/P2P
	Security	WPA/WPA2/WPA2-Enterprise/WPS
	Encryption	AES/RSA/ECC/SHA
	Firmware Upgrade	UART Download / OTA (via network) / download and write firmware via host

	Ssoftware Development	Supports Cloud Server Development / SDK for custom firmware development
	Network Protocols	IPv4, IPv6, SSL, TCP/UDP/HTTP/FTP/MQTT
	User Configuration	AT instruction set, cloud server, Android/iOS App

Note:

* ESP-32S with high temperature range option (-40°C ~ 125°C) is available for custom order.

2. Pin Definitions

2.1 Pin Layout

Figure 1: Top and Side View of ESP-32S

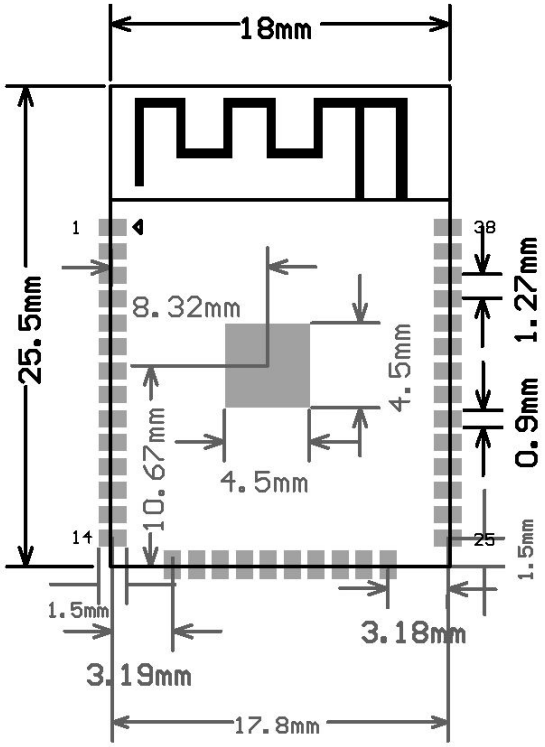


Table 2: ESP-32S Dimensions

Length	Width	Height	PAD Size(Bottom)	Pin Pitch	Shielding can height	PCB thickness
18mm	25.5mm	2.8 ± 0.1 mm	0.45 mm x 0.9 mm	1.27mm	2 mm	0.8 ± 0.1 mm

2.2 Pin Description

ESP-32S has 38 pins. See pin definitions in Table 3.

Table 3 Pin Descriptions

NO	Pin Name	Function
1	GND	Ground
2	3V3	Power supply
3	EN	Chip-enable signal. Active high
4	SENSOR_VP	GPI36, SENSOR_VP, ADC_H, ADC1_CH0, RTC_GPIO0
5	SENSOR_VN	GPI39, SENSOR_VN, ADC1_CH3, ADC_H, RTC_GPIO3
6	IO34	GPI34, ADC1_CH6, RTC_GPIO4
7	IO35	GPI35, ADC1_CH7, RTC_GPIO5
8	IO32	GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9
9	IO33	GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8
10	IO25	GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0
11	IO26	GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1

12	IO27	GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV
13	IO14	GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2
14	IO12	GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3
15	GND	Ground
16	IO13	GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER
17	SHD/SD2	GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD
18	SHD/SD3	GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD
19	SCS/CMD	GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS
20	SCK/CLK	GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS
21	SDO/SD0	GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS
22	SDI/SD1	GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS
23	IO15	GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3
24	IO2	GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0
25	IO0	GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK
26	IO4	GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPIHD, HS2_DATA1,

		SD_DATA1, EMAC_TX_ER
27	IO16	GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT
28	IO17	GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180
29	IO5	GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK
30	IO18	GPIO18, VSPICLK, HS1_DATA7
31	IO19	GPIO19, VSPIQ, U0CTS, EMAC_TXD0
32	NC	-
33	IO21	GPIO21, VSPIHD, EMAC_TX_EN
34	RXD0	GPIO3, U0RXD, CLK_OUT2
35	TXDO	GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2
36	IO22	GPIO22, VSPIWP, U0RTS, EMAC_TXD1
37	IO23	GPIO23, VSPID, HS1_STROBE
38	GND	Ground

2.3 Strapping Pins

ESP32 has 6 strapping pins.Software can read the value of these 6 bits from register ”GPIO_STRAPPING”. During the chip power-on reset, the latches of the strapping pins sample the voltage level as strapping bits of ”0”or ”1”, and hold these bits until the chip is powered down or shut down.

Each strapping pin is connected with its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impendence, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or apply the hostMCU’s GPIOs to control the voltage level of these pins when powering on ESP32.

After reset, the strapping pins work as the normal functions pins.

Refer to Table 4 for detailed boot modes configuration by strapping pins.

Table 4: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3V		1.8V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Flash Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don’t-care		0	
Debugging Log on U0TXD During Booting					
Pin	Default	U0TXD Toggling		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	Falling-edge Input Falling-edge Output	Falling-edge Input Rising-edge Output	Rising-edge Input Falling-edge Output	Rising-edge Input Rising-edge Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

Note:

Firmware can configure register bits to change the settings of ”Voltage of Internal LDO (VDD_SDIO)” and ”Timing of SDIO
Slave” after booting

3. Functional Description

This chapter describes the modules and functions implemented in ESP-32S

3.1 CPU and Internal Memory

ESP32 contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

• 448 KBytes ROM for booting and core functions.

• 520 KBytes on-chip SRAM for data and instruction.

• 8 KBytes SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.

• 8 KBytes SRAM in RTC, which is called RTC FAST Memory and can be used for data storage and accessed by the main CPU during RTC Boot from the Deep-sleep mode.

• 1 Kbit of EFUSE, of which 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including Flash-Encryption and Chip-ID.

3.2 External Flash and SRAM

ESP32 supports 4 x 16 MBytes of external QSPI flash and SRAM with hardware encryption based on AES to protect developer’s programs and data.

ESP32 accesses external QSPI flash and SRAM by the high-speed caches. Up to 16 MBytes of external flash are memory mapped into the CPU code space, supporting 8, 16 and 32-bit access. Code execution is supported. Up to 8 MBytes of external SRAM are memory mapped into the CPU data space,

supporting 8, 16 and 32-bit access. Data read is supported on the flash and SRAM. Data write is supported on the SRAM.

3.3 Crystal Oscillators

The frequencies of the main crystal oscillator supported include 40 MHz, 26 MHz and 24 MHz. The accuracy of crystal oscillators applied should be ±10 PPM, and the operating temperature range -40°C to 85°C.

When using the downloading tools, remember to select the right crystal oscillator type. In circuit design, capacitors C1 and C2 that connect to the earth, are added to the input and output terminals of the crystal oscillator respectively.The values of the two capacitors can be flexible, ranging from 6 pF to 22 pF. However, the specific capacitive values of C1 and C2 depend on further testing and adjustment of the overall performance of the whole circuit. Normally, the capacitive values of C1 and C2 are within 10 pF if the crystal oscillator frequency is 26 MHz, while 10 pF<C1 and C2<22 pF if the crystal oscillator frequency is 40 MHz.

The frequency of the RTC crystal oscillator is typically 32 kHz or 32.768 kHz. The accuracy can be out of the range of ±20 PPM, since the internal calibration is applied to correct the frequency offset. When the chip operates in low power modes, the application chooses the external low speed (32 kHz) crystal clock rather than the internal RC oscillators to achieve the accurate wakeup time.

3.4 Power Consumption

With the advanced power management technology, ESP32 can switch between different power modes as follows:

• Power mode
– Active mode: chip radio is powered on. The chip can receive, transmit, or listen.
– Modem-sleep mode: the CPU is operational and the clock is configurable. Wi-Fi / Bluetooth baseband and radio are disabled.
– Light-sleep mode: the CPU is paused. The RTC and ULP-coprocessor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip.
– Deep-sleep mode: Only RTC is powered on. Wi-Fi and Bluetooth connection data are stored in RTC memory. The ULP-coprocessor can work.
– Hibernation mode: The internal 8MHz oscillator and ULP-coprocessor are disabled. The RTC recovery memory are power-down. Only one RTC timer on the slow clock and some RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

• Sleep Pattern
– Association sleep pattern: The power mode switches between the active mode and Modem-sleep/Lightsleep mode during this sleep pattern. The CPU, Wi-Fi, Bluetooth, and radio wake up at pre-determined intervals to keep Wi-Fi / BT connections alive.
– ULP sensor-monitored pattern: The main CPU is in the Deep-sleep mode. The ULP co-processor does sensor measurements and wakes up the main system, based on the measured data from sensors.
The power consumption varies with different power modes/sleep patterns and work status of functional modules(see Table 5).

Table 5: Power Consumption by Power Modes

Power mode	Comment	Power consumption
Active mode (RF working)	Wi-Fi Tx packet 13 dBm ~ 21 dBm	160 ~ 260 mA
	Wi-Fi / BT Tx packet 0 dBm	120 mA
	Wi-Fi / BT Rx and listening	80 ~ 90 mA
	Association sleep pattern (by Lightsleep)	0.9 mA@DTIM3, 1.2 mA@DTIM1
Modem-sleep mode	The CPU is powered on.	Max speed: 20 mA
		Normal: 5 ~ 10 mA
		Slow speed: 3 mA
Light-sleep mode	-	0.8 mA
Deep-sleep mode	The ULP-coprocessor is powered on	0.15 mA
	ULP sensor-monitored pattern	25 μA @1% duty
	RTC timer + RTC memories	20 μA
Hibernation mode	RTC timer only	2.5 μA

3.5 Peripheral Interface Description

Table 6: Interface Description

Interface	Signal	Pin	Function
ADC	ADCI_CH0	SENSOR_VP	Two 12-bit SAR ADCs
	ADC1_CH3	SENSOR_VN	
	ADC1_CH4	IO32	
	ADC1_CH5	IO33	
	ADC1_CH6	IO34	
	ADC1_CH7	IO35	
	ADC2_CH0	IO4	
	ADC2_CH1	IO0	
	ADC2_CH2	IO2	
	ADC2_CH3	IO15	
	ADC2_CH4	IO13	
	ADC2_CH5	IO12	
	ADC2_CH6	IO14	
	ADC2_CH7	IO27	
	ADC2_CH8	IO25	
	ADC2_CH9	IO26	
Ultra Low Noise Analog Pre-Amplifier	SENSOR_VP	IO36	Provides about 60dB gain by using large capacitors on PCB
	SENSOR_VN	IO39	
DAC	DAC_1	IO25	Two 8-bit DACs
	DAC-2	IO26	
Touch Sensor	TOUCH0	IO4	Capacitive touch sensors
	TOUCH1	IO0	
	TOUCH2	IO2	
	TOUCH3	IO15	
	TOUCH4	IO13	
	TOUCH5	IO12	
	TOUCH6	IO14	
	TOUCH7	IO27	

	TOUCH8	IO33	
	TOUCH9	IO32	
SD / SDIO / MMC Host Controlle	HS2_CLK	MTMS	Supports SD memory card V3.01 standard
	HS2_CMD	MTDO	
	HS2_DATA0	IO2	
	HS2_DATA1	IO4	
	HS2_DATA2	MTDI	
	HS2_DATA3	MTCK	

Interface	Signal	Pin	Function
Motor PWM	PWM0_OUT0~2	Any GPIO	Three channels of 16-bit timers generate PWM waveforms; each has a pair of output signals. Three fault detection signals. Three even capture signals. Three sync signals.
	PWM1_OUT_IN0~2		
	PWM0_FLT_IN0~2		
	PWM1_FLT_IN0~2		
	PWM0_CAP_IN0~2		
	PWM1_CAP_IN0~2		
	PWM0_SYNC_IN0~2		
	PWM1_SYNC_IN0~2		
LED PWM	ledc_hs_sig_out0~7	Any GPIO	16 independent channels @80MHz clock/RTC CLK. Duty accuracy: 16bits
	ledc_ls_sig_out0~7		
UART	U0RXD_in	U2RTS_out	Two UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1TXD_out		
	U1RTS_out		
	U2RXD_in		
	U2CTS_in		

	U2TXD_out		
	U2RTS_out		
I2C	I2CEXT0_SCL_in	Any GPIO	Two I2C devices in slave or master modes
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		

Interface	Signal	Pin	Function
I2S	I2S0I_DATA_in0~15	Any GPIO	Stereo input and output from/to the audio codec, and parallel LCD data output
	I2S0O_BCK_in		
	I2S0O_WS_in		
	I2S0I_BCK_in		
	I2S0I_WS_in		
	I2S0I_H_SYNC		
	I2S0I_H_SYNC		
	I2S0I_H_ENABLE		
	I2S0O_BCK_out		
	I2S0O_WS_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		
	I2S0O_DATA_out0~23		
	I2S1I_DATA_in0~15		
	I2S1O_BCK_in		
	I2S1O_WS_in		
	I2S1I_BCK_in		
	I2S1I_WS_in		
	I2S1I_H_SYNC		
	I2S1I_V_SYNC		
	I2S1I_H_ENABLE		
	I2S1O_BCK_out		
	I2S1O_WS_out		
	I2S1I_BCK_out		
	I2S1I_WS_out		
	I2S1O_DATA_out0~23		
Remote Controller	RMT_SIG_IN0~7	Any GPIO	Eight channels of IR transmitter and receiver for various waveforms
	RMT_SIG_OUT0~7		

Interface	Signal	Pin	Function
Parallel QSPI	SPIHD	SHD/SD2	Supports Standard SPI, Dual SPI, and Quad SPI that can be connected to the external flash and SRAM
	SPIWP	SWP/SD3	
	SPICS0	SCS/CMD	
	SPICLK	SCK/CLK	
	SPIQ	SDO/SD0	
	SPID	SDI/SD1	
	HSPICLK	IO14	
	HSPICS0	IO15	
	HSPIQ	IO12	
	HSPID	IO13	
	HSPIHD	IO4	
	HSPIWP	IO2	
	VSPICLK	IO18	
	VSPICS0	IO5	
	VSPIQ	IO19	
	VSPID	IO23	
	VSPIHD	IO21	
	VSPIWP	IO22	
General Purpose SPI	HSPIQ_in/_out	Any GPIO	Standard SPI consists of clock, chip-select, MOSI and MISO. These SPIs can be connected to LCD and other external devices. They support the following features: (a) both master and slave modes; (b) 4 sub-modes of the SPI format transfer that depend on the clock phase (CPHA) and clock polarity (CPOL) control.; (c) CLK frequencies by a divider; (d) up to 64byte FIFO and DMA.
	HSPID_in/_out		
	HSPICLK_in/_out		
	HSPI_CS0_in/_out		
	HSPI_CS1_out		
	HSPI_CS2_out		
	VSPIQ_in/_out		
	VSPID_in/_out		
	VSPICLK_in/_out		
	VSPI_CS0_in/_out		
	VSPI_CS1_out		
	VSPI_CS2_out		
JTAG	MTDI	IO12	
	MTCK	IO13	
	MTMS	IO14	

	MTDO	IO15	JTAG for software debugging

Interface	Signal	Pin	Function
SDIO Slave	SD_CLK	IO6	SDIO interface that conforms to the industry standard SDIO 2.0 card specification.
	SD_CMD	IO11	
	SD_DATA0	IO7	
	SD_DATA1	IO8	
	SD_DATA2	IO9	
	SD_DATA3	IO10	
EMAC	EMAC_TX_CLK	IO0	Ethernet MAC with MII/RMII interface
	EMAC_RX_CLK	IO5	
	EMAC_TX_EN	IO21	
	EMAC_TXD0	IO19	
	EMAC_TXD1	IO22	
	EMAC_TXD2	IO14	
	EMAC_TXD3	IO12	
	EMAC_RX_ER	IO13	
	EMAC_RX_DV	IO27	
	EMAC_RXD0	IO25	
	EMAC_RXD1	IO26	
	EMAC_RXD2	TXD	
	EMAC_RXD3	IO15	
	EMAC_CLK_OUT	IO16	
	EMAC_CLK_OUT_180	IO17	
	EMAC_TX_ER	IO4	
	EMAC_MDC_out	Any GPIO	
	EMAC_MDI_in	Any GPIO	
	EMAC_MDO_out	Any GPIO	
	EMAC_CRS_out	Any GPIO	
	EMAC_COL_out	Any GPIO	

Note:

Functions of Motor PWM, LED PWM, UART, I2C, I2S, general purpose SPI and Remote Controller can be configured to any GPIO.

4. Electrical Characteristics

Note:

The specifications in this chapter are tested with general condition: V*B AT*= 3.3V, T*A*= 27°C, unless otherwise specified.

4.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

Rating	Condition	Value	Unit
Storage temperatue		-40 ~ 85	℃
Maximum soldering temperature		260	℃
Maximum soldering temperature	IPC/JEDEC J-STD-020	+2.2 ~ +3.6	V

4.2 Recommended Operating Conditions

Table 8: Recommended Operating Conditions

Operating condition	Symbol	Min	Typ	Max	Unit
Operating temperature	-	-40	20	85	℃
Supply voltage	VDD	2.2	3.3	3.6	V

4.3 Digital Terminal Characteristics

Table 9: Digital Terminal Characteristics

Terminals	Symbol	Min	Typ	Max	Unit
Input logic level low	V*I L*	-0.3	-	0.25VDD	V
Input logic level high	V*I H*	0.75VDD	-	VDD+0.3	V
Output logic level low	V*O L*	N	-	0.1VDD	V
Output logic level high	V*O H*	0.8VDD	-	N	V

4.4 Wi-Fi Radio

Table 10: Wi-Fi Radio Characteristics

Description	Min	Typical	Max	Unit
General Characteristics				
Input frequency	2412	-	2484	MHz
Input impedance	-	50	-	Ω
Input reflection	-	-	-10	dB
Output power of PA	15.5	16.5	21.5	dBm
Sensitivity				
DSSS, 1 Mbps	-	-98	-	dBm
CCK, 11 Mbps	-	-90	-	dBm
OFDM, 6 Mbps	-	-93	-	dBm
OFDM, 54 Mbps	-	-75	-	dBm
HT20, MCS0	-	-93	-	dBm
HT20, MCS7	-	-73	-	dBm
HT40, MCS0	-	-90	-	dBm
HT40, MCS7	-	-70	-	dBm
MCS32	-	-91	-	dBm
Adjacent Channel Rejection				
OFDM, 6 Mbps	-	37	-	dB
OFDM, 54 Mbps	-	21	-	dB
HT20, MCS0	-	37	-	dB
HT20, MCS7-	-	20	-	dB

4.5 Bluetooth LE Radio

4.5.1 Receiver

Table 11: Receiver Characteristics - BLE

Parameter	Condition	Min	Typ	Max	Unit
Sensitivity @0.1% BER	-	-	-98	-	dBm
Sensitivity @0.1% BER	-	0	-	-	dBm
Co-channel C/I	-	-	+10	-	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-5	-	dB
	F = F0 + 2 MHz	-	-25	-	dB
	F = F0 - 2 MHz	-	-35	-	dB
	F = F0 + 3 MHz	-	-25	-	dB
	F = F0 - 3 MHz	-	-45	-	dB
Out-of-band blocking performance	30 MHz - 2000 MHz	-10	-	-	dBm
	2000 MHz - 2400 MHz	-27	-	-	dBm
	2500 MHz - 3000 MHz	-27	-	-	dBm
	3000 MHz - 12.5 GHz	-10	-	-	dBm
Intermodulation	-	-26	-	-	dBm

4.5.2 Transmit

Table 12: Transmit Characteristics - BLE

Parameter	Condition	Min	Typ	Max	Unit
RF transmit power	-	-	+7.5	+10	dBm
RF power control range	-	-	25	-	dB
Adjacent channel transmit power	F = F0 + 1 MHz	-	-14.6	-	dBm
	F = F0 - 1 MHz	-	-12.7	-	dBm
	F = F0 + 2 MHz	-	-44.3	-	dBm
	F = F0 - 2 MHz	-	-38.7	-	dBm
	F = F0 + 3 MHz	-	-49.2	-	dBm
	F = F0 - 3 MHz	-	-44.7	-	dBm
	F = F0 + > 3 MHz	-	-50	-	dBm
	F = F0 - > 3 MHz	-	-50	-	dBm
Δf1avg	-	-	-	265	kHz
Δf2max	-	247	-	-	kHz
Δf2avg/Δf1avg	-	-	-0.92	-	kHz/50us
ICFT	-	-	-10	-	kHz
Drift rate	-	-	0.7	-	
Drift	-	-	2	-	kHz

4.6 Reflow Profile

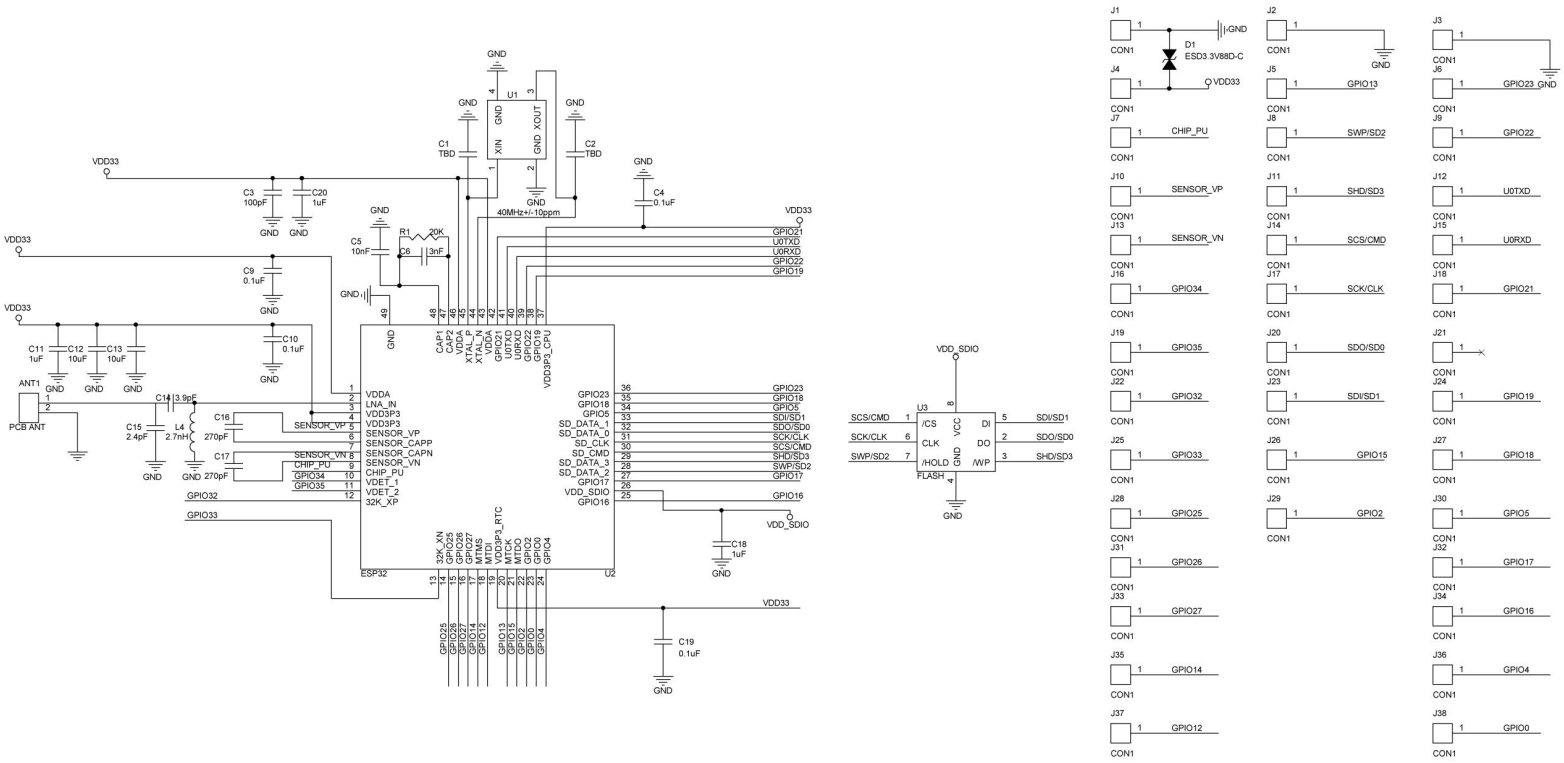
Table 13: Reflow Profile

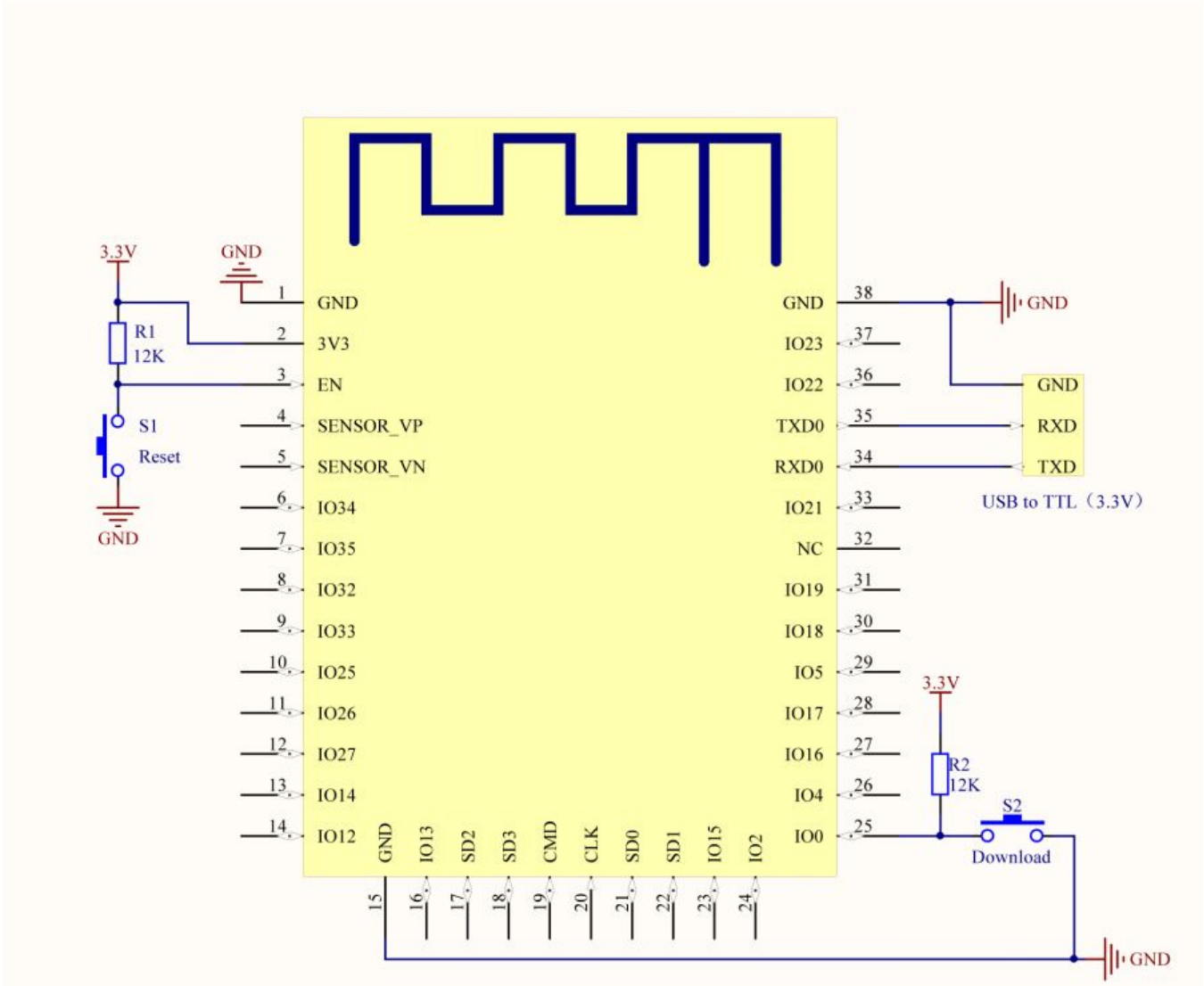
Item	Value
T*s* max to TL (Ramp-up Rate)	3°C/second max
Preheat Temperature Min. (T*s* Min.) Temperature Typ. (T*s* Typ.) Temperature Min. (T*s* Max.) Time (T*s*)	 150°C 175°C 200°C 60 ~ 180 seconds
Ramp-up rate (T*L* to T*P*)	3°C/second max
Time maintained above: –Temperature (T*L*)/Time (T*L*)	217°C/60 ~ 150 seconds
Peak temperature (T*P*)	260°C max, for 10 seconds
Target peak temperature (T*P* Target)	260°C +0/-5°C
Time within 5°C of actual peak (t *P*)	20 ~ 40 seconds
T*S* max to T*L*(Ramp-down Rate)	6°C/second max
Tune 25°C to Peak Temperature (t)	8 minutes max

Note:

The 32 kHz crystal is internally connected to ESP32's GPIO32 and GPIO33. To use ADC, Touch or GPIO functions of
IO32 and IO33, please remove the 32 kHz crystal and its capacitors — C13 and C17, and solder the 0ohm resistors —
R5 and R6.

5. Schematics





※：注意模块的供电一定要充足，最好独立供电，记得共地！

Produced by Mars 2016-10-10

EN and GPIO pins of module connection to DTR and RTS of the serial port chip, enabling software control operating mode.